REMARKS/ARGUMENTS

Claim Rejections – 35 USC § 103

Claims 10, 11, 22 and 23 were rejected under 35 U.S.C 103 (a) as being unpatentable over Flannagan (U.S. 6,031,408) and further in view of Li (U.S. 6,836,160).

Claim 10:

As pointed out by the Examiner, Flannagan (U.S. 6,031,408) FIG. 6 does not disclose "a resistor connected between a source terminal of said second transistor and ground" in a clamping circuit, as recited in Claim10. However, contrary to the Examiner's implication, Li (U.S. 6,836,160) does not teach or suggest the addition of such resistor in such a clamping circuit. (Moreover, applicant's claimed invention was conceived prior to the Nov. 19, 2002, filing date of Li; so, applicant can "swear back of" the Li reference, if called upon to do so.)

Li does not disclose a clamping circuit and does not use a current mirror in a closed feedback loop configuration. In Li, the configuration is open and the collector of the first transistor (Q2) is tied to a supply voltage source and does not connect to the collector of the output transistor (Q1). Whereas, characteristic of closed loop clamping circuits, the circuit of Applicant's Claim 10 has "a drain terminal of said third transistor is connected to a source terminal of said first transistor."

Well-known references for current mirrors, such as Gray & Meyer's "Analysis and Design of Analog Integrated Circuits," teach the addition of a resistor between a source terminal and ground of the output leg transistor of a non-clamping current mirror circuit (as, for example, in a Widlar current mirror). This is done to

increase the impedance and reduce variations on generated current on the output leg.

Li, on the other hand, adds a resistor between a source terminal and ground on the input leg of a non-clamping current mirror circuit, but for a different purpose. The purpose in Li is to cause the generation of a particular kind of reference current. The Li resistor (R1) (see, Li FIG. 3 and text , for example, at col. 1, line 65 – col. 2, line 17) enables a PTAT-type (proportional to absolute temperature) current to be mirrored to the output, which otherwise would be a CTAT-type (complementary to absolute temperature) current without the existence of that resistor. This does not provide motivation to add a resistor between transistor (135) and ground in Flannagan's FIG. 6.

The "resistor connected between a source terminal of said second transistor and ground" in the clamping circuit recited in Claim 10 enables the reduction of the size of the third transistor to reduce the parasitic capacitance on the clamped node (see, for example, Applicant's specification page 30, lines 1 - 13). Lower parasitic capacitance offers advantages such as reducing the distortion to the signal traversing the clamped node for better signal quality.

Accordingly, Li adds nothing to bring Flanagan closer to Applicant's claimed invention; and it is respectfully submitted that Claim 10 is patentable over the cited art.

Claims 11, 22 and 23:

The Examiner rejected Claims 11, 22 and 23 for similar reasons, as the rejection of Claim 10. Those claims are, accordingly, patentable for the same reasons set forth above with respect to Claim 10.

Allowable Subject Matter

Applicant thanks the Examiner for allowing Claims 6, 7, 18 and 19. Claims 6, 18 have been amended to delete the words "substantial amount of" which are an unnecessary limitation and not required for patentability. The same change applies to Claims 7, 19 which are dependent on Claims 6, 18, respectively.

Respectful request is made for reconsideration of the application, as amended, and for an issuance of a Notice of Allowance.

Respectfully submitted,

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